CMOS SENSOR CAMERA
WITH ON-CHIP IMAGE COMPRESSION

ABSTRACT OF THE DISCLOSURE

A digital camera (10) that has an array (11) of CMOS sensor elements (11a). The array (11) is read in a manner that performs spatial-to-frequency transforms for image compression on the analog output signals of the sensor elements. More specifically, wordlines (12) and bitlines (13) are pulsewidth modulated so that the coincidence of their "on" times corresponds to a desired coefficient of the basis function of the transform (FIGUREs 3 and 4). Additional comparator circuitry (15), quantizers (16), and encoding circuitry (19) can be part of the same integrated circuit as the array (11).